AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A phase locked loop (PLL) circuit having a receiver voltage controlled oscillator (VCO), a transmitter VCO, and a crystal oscillator, the PLL circuit comprising:

a control circuit for generating a reference control signal in response to a reception enable signal and a transmission enable signal;

a reception divider for receiving a reception division data signal in response to the reception enable signal and dividing an output signal of the receiver VCO according to the reception division data signal;

a reference divider for receiving a reference division data signal in response to the reference control signal of the control circuit and dividing the output signal of ~~a~~ the crystal oscillator according to the reference division data signal;

a transmission divider for receiving a transmission division data signal in response to the transmission enable signal and dividing an output signal of the transmitter VCO according to the transmission division data signal;

a first phase detector for detecting frequency and phase differences between an output signal of the reception divider and an output signal of the reference divider; and

a second phase detector for detecting the frequency and phase differences between an output signal of the transmission divider and the output signal of the reference divider.

2. (Original) The phase locked loop circuit of claim 1, wherein the control circuit comprises an apparatus for performing a logic OR operation on the reception enable signal and the transmission enable signal.

3. (Currently Amended) The phase locked loop circuit of claim 1, wherein the reception divider comprises:

a first switch for ~~switching~~ gating the reception division data signal in response to the reception enable signal; and

a reception counter for dividing the output signal of the receiver VCO in response to an output signal of the first switch.

4. (Currently Amended) The phase locked loop circuit of claim 1, wherein the reference divider comprises:

a second switch for ~~switching~~ gating the reference division data signal in response to the reference control signal of the control circuit; and

a reference counter for dividing the output signal of the crystal oscillator in response to an output signal of the second switch.

5. (Currently Amended) The phase locked loop circuit of claim 1, wherein the transmission divider comprises:

a third switch for ~~switching~~ gating the transmission division data signal in response to the transmission enable signal; and

a transmission counter for dividing the output signal of the transmitter VCO in response to an output signal of the third switch.

6. (Original) The phase locked loop circuit of claim 1, further comprising:

a latch for receiving serial data signals and outputting the reception division data signal, the reference division data signal, the transmission division data signal, the reception enable signal, the reference enable signal and the transmission enable signal.

7. (Original) The phase locked loop circuit of claim 3, wherein the first switch is an NMOS transistor.

8. (Original) The phase locked loop circuit of claim 3, wherein the first switch is a transmission gate.

9. (Original) A phase locked loop circuit having a receiver voltage controlled oscillator (VCO), a transmitter VCO, and a crystal oscillator, the PLL circuit comprising:

a control circuit for outputting a reception control signal and a transmission control signal in response to a reception enable signal, and a transmission enable signal;

a reception divider for receiving a reception division data signal in response to the reception control signal and dividing an output signal of the receiver VCO according to the reception division data signal;

a reference divider for receiving a reference division data signal in response to a reference enable signal and dividing an output signal of the crystal oscillator according to the reference division data signal;

a transmission divider for receiving a transmission division data signal in response to the transmission control signal of the control circuit and dividing an output signal of the transmitter VCO according to the transmission division data signal;

a first phase detector for detecting frequency and phase differences between an output signal of the reception divider and an output of the reference divider; and

a second phase detector for detecting the frequency and phase differences between an output signal of the transmission divider and an output signal of the reference divider.

10. (Original) The phase locked loop circuit of claim 9, wherein the control circuit comprises:

a first inverter for inverting a phase of the reception enable signal;

a second inverter for inverting a phase of the transmission enable signal;

a first flip-flop having a clock terminal, an input terminal, and a reset terminal, to which is respectively applied an output signal of the reference divider, a power voltage, and an output signal of the first inverter, and having an output terminal that outputs the reception control signal; and

a second flip-flop having a clock terminal, an input terminal, and a reset terminal, to which is respectively applied an output signal of the reference divider, a power

voltage, an output signal of the second inverter, and having an output terminal that outputs the transmission control signal.

11. (Currently Amended) The phase locked loop circuit of claim 9, wherein the reception divider comprises:

a first switch for ~~switching~~ gating the reception division data signal in response to the reception control signal of the control circuit; and

a reception counter for dividing the output signal of the receiver VCO in response to an output signal of the first switch.

12. (Currently Amended) The phase locked loop circuit of claim 9, wherein the reference divider comprises:

a second switch for ~~switching~~ gating the reference division data signal in response to the reference enable signal; and

a reference counter for dividing the output signal of the crystal oscillator in response to an output signal of the second switch.

13. (Currently Amended) The phase locked loop circuit of claim 9, wherein the transmission divider comprises:

a third switch for ~~switching~~ gating the transmission division data signal in response to the transmission control signal of the control circuit; and

a transmission counter for dividing the output signal of the transmitter VCO in response to an output signal of the third switch.

14. (Original) The phase locked loop circuit of claim 9, further comprising:

a latch for receiving serial data signals and outputting the reception division data signal, the reference division data signal, the transmission division data signal, the reception enable signal, the reference enable signal and the transmission enable signal.

15. (Original) The phase locked loop circuit of claim 11, wherein the first switch is an NMOS transistor.

16. (Original) The phase locked loop circuit of claim 11, wherein the first switch is a transmission gate.